REMARKS

In an Office Action mailed on June 28, 2005, an objection was made to claim 27; claims 1-9 and 16-28 were rejected under 35 U.S.C. § 112, first paragraph; claims 1-3, 7, 10, 11, 15-17 and 22 were rejected under 35 U.S.C. § 102(e) as being anticipated by Dvorak; and claims 4-6, 8, 9, 12-14, 18-21, 23 and 24-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dvorak in view of Silvestri. Claim 27 has been amended to overcome the corresponding objection. The §§ 102, 103 and 112 rejections are addressed below.

§ 112 Rejections:

Claims 1-9 and 16-28 stand rejected under 35 U.S.C. § 112, first paragraph as allegedly failing to comply with the written description requirement.

As amended, the specification now explicitly recites language from the originally-filed claims, which may be considered part of the original disclosure. Thus, as amended, the specification recites an embodiment that includes a system that includes a locked loop circuit and a processor that is coupled to the locked loop circuit to control the locked loop circuit and perform at least one other function in the system that is not related to the control of the locked loop circuit. The specification has also been amended to recite an embodiment in which a method includes providing a locked loop circuit that has a processor accessible interface and using a processor to control the locked loop circuit and perform at least one other function not related to the control of the locked loop circuit.

The specification amendments do not introduce any new matter.

Therefore, for at least the reason that the newly-added paragraphs contain a written description of independent claims 1 and 16, withdrawal of the § 112, first paragraph rejections is requested.

Applicant requests withdrawal of the § 112, first paragraph rejections for at least the additional, independent reason that on page 2, the specification states that the microprocessor may form a central processing unit (CPU) for the computer system 10. Thus, this statement alone supports claims 1 and 16, in that a microprocessor 12 is described that may perform a function, (i.e., a function related to being a CPU of a computer system) other than a function related to controlling a locked loop circuit. Furthermore, on page 2 of the specification, the specification recites that the microprocessor 12 interacts with many components of the computer system such as a north bridge, or memory hub 16 and a memory 20 that forms at least part of the

overall system memory for the computer system 10. Therefore, these are additional functions that are performed by the microprocessor 12, which are not related to the control of a locked loop circuit.

Thus, for at least the reasons that are set forth above, withdrawal of the § 112, first paragraph rejections of claims 1-9 and 16-28 is requested.

§§ 102 and 103 Rejections of Claims 1-9:

The system of independent claim 1 recites a locked loop circuit and a processor that is coupled to the locked loop circuit to control the locked loop circuit and perform at least one other function in the system not related to the control of the locked loop circuit.

In the rejection of independent claim 1, the Examiner refers to the processor 105 of Dvorak and to the various figures of Dvorak that show delay locked loops (DLLs) and phase locked loops (PLLs). However, Dvorak fails to teach or suggest that the processor 105 controls any of the DLLs or PLLs. As such, Dvorak fails to anticipate independent claim 1.

Claims 2-9 are patentable for at least the reason that these claims depend from an allowable claim. Therefore, for at least the reasons that are set forth above, withdrawal of the §§ 102 and 103 rejections of claims 1-9 is requested.

§§ 102 and 103 Rejections of Claims 10-15:

The locked loop circuit of independent claim 10 includes an interface that is accessible by a processor to control a locked loop circuit to adjust a timing between an input clock signal and an output clock signal. Applicant requests the Examiner to specifically point out the alleged interface of Dvorak's system. In this regard, Dvorak discloses a feedback network 315 but there is no discussion or even a suggestion in Dvorak that the feedback network 315 is somehow controlled by the processor 105. Rather, Dvorak is specific that the phase detector 310 controls the feedback network 315. *See, for example,* Dvorak, 4:1-9.

Claims 11-15 are patentable for at least the reason that these claims depend from an allowable claim. Therefore, for at least the reasons that are set forth above, withdrawal of the §§ 102 and 103 rejections of claims 10-15 is requested.

§§ 102 and 103 Rejections of Claims 16-23:

The method of independent claim 16 includes providing a locked loop circuit that has a processor accessible interface. The method includes using a processor to control the locked loop circuit and perform at least one other function not related to the control of the locked loop circuit.

See discussion of independent claims 1 and 10 above. In particular, Dvorak neither teaches nor suggests a processor accessible I nterface of a locked loop circuit and neither teaches nor suggests a processor to control a locked loop circuit and perform at least one other function not related to the control of the locked loop circuit. Thus, the feedback network 315 of Dvorak is controlled by the phase detector 310 and not by a processor. Furthermore, there is no teaching or suggestion in Dvorak that the processor 105 controls one of disclosed DLLs or PLLs.

Claims 17-23 are patentable for at least the reason that these claims depend from an allowable claim. Therefore, for at least the reasons that are set forth above, withdrawal of the §§ 102 and 103 rejections of claims 16-23 is requested.

§ 103 Rejections of Claims 24-28:

The article of independent claim 24 includes a computer accessible storage medium that stores instructions to, when executed, cause a processor-based system to control a locked loop circuit. The processor performs at least one other function not related to the control of the locked loop circuit.

See discussion of independent claims 1, 10 and 16 above. In particular, Dvorak neither teaches nor suggests instructions to cause a processor to control a locked loop circuit, wherein the processor performs at least one other function not related to the control of the locked loop circuit. Therefore, for at least this reason, Dvorak fails to teach or suggest the instructions of independent claim 24, Silvestri fails to teach or suggest the missing claim limitations. Therefore, a *prima facie* case of obviousness has not been established for claim 24, in that the hypothetical combination of Dvorak and Silvestri fails to teach all limitations of claim 24.

Claims 25-28 are patentable for at least the reason that these claims depend from an allowable claim. Therefore, for at least the reasons that are set forth above, withdrawal of the §§ 102 and 103 rejections of claims 24-28 is requested.

CONCLUSION

In view of the foregoing, withdrawal of the §§ 102, 103 and 112 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0550US).

Respectfully submitted,

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